

**ELECTRICAL SPECIFICATION**

Output Logic Parameter	PECL		LVDS		Unit
	Min.	Max.	Min.	Max.	
	3.3		3.3		
Supply Voltage Variation(V _{DD}) 10%	2.97	3.63	2.97	3.63	V
Frequency Range	100	700	100	700	MHz
Standard Frequency	122.88, 125, 155.52, 200, 300, 350, 400, 491.52, 622.08, 625				MHz
Operating Temp. Range	Refer to Ordering Information				°C
Frequency Stability *	Refer to Ordering Information				ppm
Pulling Range	±100	–	±100	–	ppm
Control Voltage Range	0.3	3.0	0.3	3.0	V
Supply Current					
100MHz ≤ Fo < 160MHz	–	75	–	65	mA
160MHz ≤ Fo ≤ 700MHz	–	100	–	80	
Output Level					
Output High (Logic “1”)	2.275	–	–	1.6	V
Output Low (Logic “0”)	–	1.68	0.9	–	
Transition Time:Rise/Fall Time †	–	1.0	–	1.0	nSec
Start Time	–	3	–	3	mSec
Tri-State					
Output Active	2.5	–	2.5	–	V
Output in High Impedance State	–	0.5	–	0.5	
Linearity	–	10	–	10	%
Modulation Bandwidth(BW)	25	–	25	–	KHz
Input Impedance	50	–	50	–	KΩ
RMS Phase Jitter (Integrated 12KHz ~ 20MHz)	–	4	–	4	pS
Storage Temp. Range	-55	125	-55	125	°C

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.

* Inclusive of calibration @ 25°C, operating temperature range, input voltage variation, load variation, aging, shock, and vibration.

† Transition times are measured between 20% and 80% waveform.

