





## ELECTRICAL SPECIFICATION

Output Logic Parameter	PECL				LVDS				Unit
	Min.		Max.		Min.		Max.		
Supply Voltage Variation(V <sub>DD</sub> ) 5%	3.3	2.5	3.3	2.5	3.3	2.5	3.3	2.5	V
Frequency Range	3.135	2.375	3.465	2.625	3.135	2.375	3.465	2.625	MHz
Standard Frequency	19.44, 76.8, 77.76, 106.25, 122.88, 125, 155.52, 156.25, 153.6, 161.1328, 200								MHz
Operating Temp. Range	Refer to Ordering Information								°C
Frequency Stability *	Refer to Ordering Information								ppm
Pulling Range	±70		-		±70		-		ppm
Control Voltage Range	0.3	0	3.0	2.5	0.3	0	3.0	2.5	V
Supply Current									
1.5MHz ≤ Fo < 65MHz	-		75		-		45		mA
65MHz ≤ Fo ≤ 200MHz	-		100		-		80		
Output Level									
Output High (Logic "1")	2.275	1.475	-		-		1.6		V
Output Low (Logic "0")	-		1.68	1.095	0.9		-		
Transition Time:Rise/Fall Time †	-		1.0		-		1.0		nSec
Start Time	-		3		-		3		mSec
Tri-State									
Output Active	-		0.5	0.5	-		0.5	0.5	V
Output in High Impedance State	2.5	2	-		2.5	2	-		
Linearity	-		10		-		10		%
Modulation Bandwidth	25		-		25		-		KHz
Input Impedance	50		-		50		-		KΩ
RMS Phase Jitter (Integrated 12KHz ~ 20MHz)	-		0.3		-		0.3		pS
Storage Temp. Range	-55		125		-55		125		°C

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.

\* Inclusive of calibration @ 25°C, operating temperature range, input voltage variation, load variation, aging, shock, and vibration.

† Transition times are measured between 20% and 80% waveform.

