





## ELECTRICAL SPECIFICATION

Output Logic Parameter	PECL				LVDS				Unit
	Min.		Max.		Min.		Max.		
Supply Voltage Variation(V <sub>DD</sub> ) 5%	3.3	2.5	3.3	2.5	3.3	2.5	3.3	2.5	V
Frequency Range	3.135	2.375	3.465	2.625	3.135	2.375	3.465	2.625	
Standard Frequency	19.44, 320, 19.44, 320								MHz
Operating Temp. Range	25, 38.88, 62.5, 77.76, 100, 106.25, 125, 155.52, 156.25, 159.375, 161.1328, 164.355469, 167.3316, 187.5, 212.5, 250, 312.5								MHz
Frequency Stability *	Refer to Ordering Information								°C
Supply Current	Refer to Ordering Information								ppm
19.44MHz ≤ Fo < 160MHz	-		75		-		50		mA
160MHz ≤ Fo < 250MHz	-		100		-		50		
250MHz ≤ Fo ≤ 320MHz	-		100		-		65		
Output Level									
Output High (Logic "1")	2.275	1.475	-		-		1.6		V
Output Low (Logic "0")	-		1.68	1.095	0.9		-		
Transition Time:Rise/Fall Time †	-		1.0		-		1.0		nSec
Start Time	-		3		-		3		mSec
Tri-State (Input to Pin 2 or Pin 1)									
Output Active	2.5	2	-		2.5	2	-		V
Output in High Impedance State	-		0.5	0.5	-		0.5	0.5	
RMS Phase Jitter (Integrated 12KHz ~ 20MHz)	-		0.3		-		0.3		pS
Storage Temp. Range	-55		125		-55		125		°C

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.

\* Inclusive of calibration @ 25°C, operating temperature range, input voltage variation, load variation, aging, shock, and vibration.

† Transition times are measured between 10% and 90% of V<sub>DD</sub>, with an output load of 15pF.