



ELECTRICAL SPECIFICATION

Output Logic Parameter	PECL		LVDS		Unit
		Max.	Min.	Max.	
	3.3		3.3		V
Supply Voltage Variation(V _{DD}) 10%	2.97	3.63	2.97	3.63	
Frequency Range	100	700	100	700	MHz
Standard Frequency	175, 200, 240, 250, 312.5, 320, 350, 622.08, 625				MHz
Operating Temp. Range	Refer to Ordering Information				°C
Frequency Stability *	Refer to Ordering Information				ppm
Supply Current					mA
100MHz ≤ Fo < 160MHz	–	75	–	65	
160MHz ≤ Fo ≤ 700MHz	–	100	–	80	
Output Level					V
Output High (Logic “1”)	2.275	–	–	1.6	
Output Low (Logic “0”)	–	1.68	0.9	–	
Transition Time:Rise/Fall Time †	–	1.0	–	1.0	nSec
Start Time	–	3	–	3	mSec
Tri-State					V
Output Active	2.5	–	2.5	–	
Output in High Impedance State	–	0.5	–	0.5	
RMS Phase Jitter (Integrated 12KHz ~ 20MHz)	–	4	–	4	pS
Storage Temp. Range	-55	125	-55	125	°C

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.

* Inclusive of calibration @ 25°C, operating temperature range, input voltage variation, load variation, aging, shock, and vibration.

† Transition times are measured between 10% and 90% of V_{DD}, with an output load of 15pF.